SuperTools Proposers’ Day Conference

SYNOPSIS

The Intelligence Advance Research Projects Activity (IARPA) will host a Proposers’ Day Conference for the SuperTools program on February 10, 2016, in anticipation of the release of a new solicitation. The Conference will be held from 9 AM to 4 PM EST in the Washington, DC metropolitan area. The purpose of the conference will be to provide information on the SuperTools program, and on the research problems the program aims to address, to address questions from potential proposers, and to provide a forum for potential proposers to present their capabilities for teaming opportunities.

This announcement serves as a pre-solicitation notice and is issued solely for information and planning purposes. The Proposers’ Day Conference does not constitute a formal solicitation for proposals or proposal abstracts. Conference attendance is voluntary and is not required to propose to future solicitations (if any) associate with this program. IARPA will not provide reimbursement for costs incurred to participate in this conference.

PROGRAM DESCRIPTION AND GOALS

As a basis for constructing ever-more powerful computers, semiconductor-based technology is reaching its scaling limits. As semiconductor-based exo-scale computing is projected to consume enormous amounts of energy, IARPA is pursuing alternative technologies. One such alternative, Superconducting Electronics (SCE), is a promising technology for digital circuits due to its high switching speed and low power consumption.

The SuperTools program aims to develop a comprehensive set of Electronic Design Automation (EDA) tools to enable Very-Large-Scale Integration (VLSI) design of Superconducting Electronics (SCE). The program seeks to enable the design and modeling of very-large-scale SCE circuits needed to build a prototype superconducting computer. SuperTools is envisioned as a five year program. The three-year goal of the SuperTools program is to develop a capability that supports the design of an Arithmetic Logic Unit (ALU), co-processors and other similar devices. The five-year goal is to support the design of a 64-bit Reduced Instruction Set Computing (RISC) microprocessor from design concept to tape-out. The SuperTools program will also develop physics-based Technology Computer Aided Design (TCAD) tools and establish Standard Cell Library templates for SCE to bridge collaboration between SCE foundries and IC designers.

The tools developed under the SuperTools program will need to handle complex designs with approximately 10M Josephson Junctions or 1M gates. The program aims to leverage existing Complementary Metal-Oxide Semiconductor (CMOS) toolchains to speed up tool development. The developed tools are desired to be applicable to all families of superconducting digital logic, as well as capable of optimizing a design based on metrics such as circuit area, power, energy per operation, or speed.

Although the high level SCE EDA (Electronic Design Automation) workflow will likely be similar to the existing CMOS EDA workflow, SCE circuit design has unique requirements imposed by superconductivity, which prevent direct porting of the existing CMOS EDA toolchain to SCE design. At present, the EDA toolchain and TCAD tools for SCE are incomplete and limited both in capability and scale. The
SuperTools program is anticipated to focus on developing EDA tools with new automation algorithm and design methodology adapted to the following differences:

1. Different representation of logic states and switch construct: SCE pulse logic vs. CMOS level logic.
3. Different timing/clocking and distribution schemes.
4. Different biasing and distribution schemes.
5. Different suites of basic logic gates and constructs.
6. Different levels of inter-gate influence: magnetic vs. electric coupling.
7. Different passive components: inductor vs. capacitor (current vs. charge).
8. Different interconnect technology: superconductor vs. normal conductor.
9. Existence of nonlogic cells: interconnects (Passive Transmission Line (PTL), Josephson Transmission Line (PTL)), asynchronous components (splitter, merger), and other special purpose circuits (SFQ/ Direct Current (DC) and DC/SFQ converters).

The SuperTools program seeks to develop tools for a complete design workflow with SCE-specific requirements in a streamlined, systematic approach:

1. Full EDA toolchain specific to SCE requirements that automates design workflow from Hardware Description Language/Register Transfer Level (HDL/RTL) to Graphic Data System (GDS) in order to reduce design cycle time, increase design reliability, and enable design of complex, very large scale digital circuits;
2. TCAD device and process simulators, parameter extraction tools, and Standard Cell Library templates to support digital and analog circuit synthesis and simulations for SCE;
3. Bringing together the SCE design and fabrication communities through a standardized exchange platform; and
4. Bridging the gap between SCE and CMOS design.

The SuperTools program will develop a comprehensive set of EDA and TCAD tools, including

1. Logic/digital design tool and HDL simulator.
2. Logic synthesis tool.
3. Clock tree and bias network synthesis tools.
4. Analog circuit schematic simulator and editor.
5. Layout synthesis tool and editor.
6. Place-and-route tool.
7. Physical design verification tools.
8. Physics-based device and process simulation tools.
9. Device and circuit parameter extraction tools.
11. Timing and power analysis tools.

The SuperTools program is divided into three phases. Phase 1 – Initial Tool Development – will run for a period of 24 months, Phase 2 – Tool Improvement – will run for a period of 24 months, followed by Phase 3 – Tool Integration and Capability Extension – which will run for 12 months.

Collaborative efforts and teaming among potential performers will be strongly encouraged. Government Test and Evaluation (T&E) teams will provide assistance in tool validation and access to foundry data when needed.
IARPA anticipates that industrial and academic institutions from around the world will participate in this program. Researchers will be encouraged to publish their findings in academic journals.

REGISTRATION INFORMATION

Attendees must register no later than 12:00 PM EST on Wednesday February 3, 2016, at http://events.SignUp4.com/SuperToolsPD_Registration. Directions to the conference facility and other materials will be available on that website. No walk-in registrations will be allowed.

The conference will be conducted at the unclassified level.

Due to space limitations, attendance will be limited to the first 100 registrants and to no more than 3 representatives per organization. All attendees will be required to present a government-issued photo identification to enter the conference. Non-US citizens will be required to submit a visit request form for Foreign Nationals at least 5 business days prior to the conference. The form and submission instructions can be found on the registration website. Foreign nationals will need to present a passport.

ADDITIONAL INFORMATION

Proposers’ Day information is found at the registration web site and should be consulted for updates.

The unclassified morning session will include an overview of the program goals, technical challenges, and expected participation requirements. A description of how the solutions will be evaluated will be provided.

The afternoon will include unclassified presentation & poster sessions to provide an opportunity for attendees to present their organizations' capabilities and to explore teaming arrangements. Attendees who wish to present organization capabilities for teaming opportunities may submit a request through the registration web site. Details on the presentation and poster formats, and the procedure for submitting a request to present, will be provided after approval to register for the conference has been granted. Time available for presentations and posters will be limited. Therefore, presentations will be limited to the first 15 registered respondents who request an oral presentation, and posters will be limited to the first 25 registered respondents who request a poster presentation. These presentations are not intended to solicit feedback from the Government, and Government personnel will not be present during the presentations.

This Proposers' Day is intended for participants who are eligible to compete on the anticipated Broad Agency Announcement (BAA). Other Government Agencies, Federally Funded Research and Development Centers (FFRDCs), University Affiliated Research Centers (UARCs), or any other similar organizations that have a special relationship with the Government, that gives them access to privileged or proprietary information, or access to Government equipment or real property, will not be eligible to submit proposals to the anticipated BAA nor participate as team members under proposals submitted by eligible entities. While such entities are not prohibited from attending the Proposers' Day, due to space limitations, preference will be given first to those organizations that are eligible to compete and
attendees from such entities will be limited to no more than 30. IARPA will not provide reimbursement for costs incurred to participate in this conference.

Questions concerning conference & registration can be sent to dni-iarpa-events@iarpa.gov.
Questions regarding the program can be sent to dni-iarpa-baa-16-03@iarpa.gov.

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