USC Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

Seminar Announcement

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Performance-Power Trade-off without DVFS: An Architecture and Runtime Joint Approach

Tuesday, April 1, 2014 at 10:30AM
Electrical Engineering Building (EEB 248)

Hosted by Prof. Murali Annavaram

Providing a sufficient voltage/frequency (V/F) scaling range is critical for effective power management. However, it has been fraught with decreasing nominal operating voltage and increasing process variability that makes it harder to scale the minimum operating voltage (VMIN). Facing such a challenge, we first propose to jointly scale (i) the resources of cores (e.g., the size of on-chip memories, the number of execution units, etc.) and (ii) the number of operating cores to maximize performance of multi-core processors under the maximum power constraint; scaling (i) is adopted as a mean to compensate for a lack of V/F scaling range while scaling (ii) is to exploit the effect of spreading threads over more or fewer cores and scaling shared resources on performance. Under the power constraint, disabling resources of each core allows us to increase the number of operating cores, and vice versa (dubbed resource and core scaling (RCS)). We demonstrate that the best RCS configuration for a given application can improve performance by 21%. Second, we propose a runtime system that predicts the best RCS configuration for a given application and adapts the processor accordingly at runtime. The runtime system only needs to examine a small fraction of runtime to predict the optimal RCS configuration with accuracy well over 90%, whereas the runtime overhead of prediction and adaptation is small.

Finally, we demonstrate that selectively scaling the re-sources in RCS (sRCS) considering on application's characteristics can offer higher performance than uniformly scaling them (i.e., RCS). sRCS can provide 6% higher performance than RCS.

Bio:
Nam Sung Kim is an Associate Professor at the University of Wisconsin-Madison. He has been conducting interdisciplinary research that cuts across device, circuit, architecture, and runtime system for power-efficient computing. His research has been supported by National Science Foundation (NSF), Semiconductor Research Corporation (SRC), Defense Advanced Research Project Agency (DARPA), BAE Systems, AMD, IBM, Samsung, and Microsoft; the total funding amount provided/pledged by these agencies is nearly 3.5 million dollars to date. Prior to joining the University of Wisconsin-Madison, he was a senior research scientist at Intel from 2004 to 2008, where he conducted research in power-efficient digital circuit and processor architecture.

Nam Sung Kim has published more than 100 refereed articles to highly-selective conferences and journals in the field of digital circuit, processor architecture, and computer-aided design. The top five most frequently cited papers have more than 2500 combined citations and the total number of combined citations of all his papers exceeds 4000 according to Google Scholar. He also has served several prominent international conferences as a technical program committee member. He was a recipient of IEEE Design Automation Conference (DAC) Student Design Contest Award in 2001, Intel Fellowship in 2002, and IEEE International Conference on Microarchitecture (MICRO) Best Paper Award in 2003, NSF CAREER Award in 2010, and IBM Faculty Award in 2011 and 2012, and he was early-tenured in 2013. His current research interest is designing robust and power-efficient computing systems. He is an IEEE senior member and holds a Ph.D. degree in Computer Science and Engineering from the University of Michigan-Ann Arbor, and both M.S. and B.S. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology.