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Taming Relaxed Memory Consistency and Non-determinism in Parallel Systems

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Electrical Engineering Building (EEB 248)

Hosted by Prof. Michel Dubois

With computer architectures moving towards an era dominated by many-core machines and the ever-increasing demands of big data processing, parallel programming has become the norm. Unfortunately, most current programmers find parallelism challenging. It is urgent to provide architectural and software supports to make parallel applications easy to build, reason and debug. Among others, relaxed memory consistency and non-determinism in particular make shared-memory based parallel programming difficult.

In this talk, I will give an overview of our strategy to tame the two factors. Specifically, I will present OmniOrder, a cache coherence protocol for atomic blocks (transactions). It eliminates the effects of relaxed consistency by supporting strict sequential consistency with high performance. OmniOrder supports conflict serialization based on the conventional directory-based protocol. I will also present Pacifier, a deterministic record and replay scheme for relaxed consistency models beyond Total-Store-Order (TSO). It helps to track and understand the behaviors of relaxed consistency.

Bio:

Xuehai Qian is a postdoctoral researcher at University of California Berkeley. He got the Ph.D. from the Department of Computer Science at the University of Illinois, Urbana-Champaign in 2013. His research interests include parallel computer architecture, architectural support for programming productivity and debugging support for large-scale HPC applications. He received an MS in Computer Science from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), and a BS in Computer Engineering from Beihang University, Beijing.