USC Viterbi School of Engineering
*Ming Hsieh Department of Electrical Engineering*

**Ming Hsieh Institute Seminar Series**
Ming Hsieh Department of Electrical Engineering

**Integrated Systems**

# Phase Noise Filter for LO Phase Noise Suppression


## Dr. Jane Gu

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Date: Friday, November 3, 2017
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**Abstract:** For many high performance electronic systems, clock phase noise is the fundamental limitation of the key specifications, for example SNR or EVM of communication systems, the resolution and speed of ADC/DAC. Low phase noise or low jitter clock generation, such as OEO or DRO, can provide superior phase noise performance, such as -160 dBc/Hz @ 1MHz offset for 1 GHz clock. However, the shoebox size prevents them to be deployed in consumer electronics, especially for portable devices. On-chip clock generation on the other hand is constrained by the large loss mechanisms, such as substrate loss, low quality factor components. Moreover, modern electronics prefer multi-band and multi-mode operations, which also requires the clock generation to be wideband or tunable. These features further compromise the clock phase noise. To address this issue, we propose delay line based phase noise cancellation technique, which aims to decouple the low phase noise requirement from wideband LO generation. In this talk, I will first introduce the concept of the proposed phase noise filter technique. After that, I will present several proof-of-concept design examples for a 10 GHz clock.


**Biography:** Dr. Qun Jane Gu has received the Ph.D. from University of California, Los Angeles in 2007. After graduation, she has worked as a senior design engineer in Wionics Realtek research group, a staff design engineer in AMCC on CMOS mm-wave and optic I/O circuits, and a postdoctoral researcher at UCLA. From August 2010 to August 2012, she joined University of Florida as an assistant professor. Since August 2012, she has been with University of California, Davis, where she is currently an associate professor. Dr. Jane Gu's research interest covers high efficiency, low power interconnect, mm-wave and sub-mm-wave/THz integrated circuits and systems and SoC design techniques based on mainstream semiconductor devices and post-CMOS devices. The target applications include communications, radar and imaging, and biosensing. She is a co-recipient of several best paper awards, 2014 IEEE WAMICON Best Conference Paper, 2015 IEEE APMC Best Student Paper, 2016 IEEE IMS Best Student Paper 2nd Place, 2016 IEEE RFIT Best Student Paper, 2017 IEEE IMS Best Student Paper 3rd Place. She has received NSF CAREER award, 2015 College of Engineering Outstanding Junior Faculty Award and 2017 Qualcomm Faculty Award.

*Hosted by Prof. Hossein Hashemi, Prof. Mike Chen, Prof. Mahta Moghaddam and Prof. Dina El-Damak. Organized and hosted by Shiyu Su.*