USC Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

Ming Hsieh Institute Seminar Series
Ming Hsieh Department of Electrical Engineering

Integrated Systems

CMOS Digital Microwave

Dr. Scott Powell

VP Engineering at Jariet Technologies

Date: Friday, March 3rd, 2017
Time: 2:30pm Location: EEB 132

Abstract: Microwave and millimeter-wave functions have traditionally been implemented by deeply experienced RF design (and test) experts using specialized distributed design techniques, discrete components, and specialized fabrication processes. Conventional wisdom has been that these functions cannot be implemented in standard, high volume digital CMOS processes. However, someone forgot to tell the analog design community that they couldn't do this in standard CMOS. Unprecedented advances in analog-to-digital (ADC) and digital-to-analog (DAC) converter techniques have combined with CMOS fabrication technology's continual ability to follow Moore's law to create smaller and faster "digital" FET transistors. Sample rates for today's shipping CMOS ADCs and DACs exceed 65Gsamples/sec (sps) with talk of >100Gsps just around the corner. This allows ADCs and DACs to be placed closer and closer to the antenna enabling traditional micro- and millimeter-wave operations like mixing, filtering, down conversion, multi-input/multi-output (MIMO) antenna channels, and beam forming to be implemented with digital techniques. In addition, once in the digital domain, operations like dual polarization, linearization, and adaptive equalization become feasible allowing much higher levels of performance and functionality than have ever been achieved with traditional microwave techniques. Applications include next generation cell phones, microwave links, wireless access, radar, satellite communication, etc.

This talk will summarize advanced CMOS process technologies and techniques for CMOS implementations of >65Gsps ADCs and DACs along with specifications typically achievable from these converters. A few "digital microwave" applications will be highlighted which are enabled by the availability of ultra-high speed data converters. Digital signal processing techniques for converting direct sampled RF spectrum to baseband signals will be discussed along with considerations for CMOS ASIC implementations. High speed analog functions follow a very different design flow than large (100M+ gate) digital design flows. This talk will conclude with a discussion of the major issues and approaches for merging high speed analog and digital design flows to create single chip, mixed-signal "digital microwave" systems-on-a-chip.

Biography: Dr. Powell has over 30 years' experience in the semiconductor industry building and leading cutting edge design teams in all aspects of complex DSP, communications systems, and high speed mixed-signal ASIC design. He earned a Ph.D. degree in Electrical Engineering from the University of California, San Diego. His accomplishments include over 60 issued and pending patents, 29 journal and conference publications, and numerous mixed signal ASIC products in high volume production. Dr. Powell has started and sold a semiconductor startup, was Sr. Director of the Ethernet PHY group at Broadcom leading a multi-national team to become the dominant market leader with over 40 tapeouts, and was VP Engineering at ClariPhy executing on a >200M gate mixed-signal coherent optical PHY ASIC going to production with A-revision silicon. Dr. Powell is most recently VP ASIC Engineering at Jariet building and leading a team to create digital microwave products.

Hosted by Prof. Hossein Hashemi, Prof. Mike Chen, Prof. Dina El-Damak, and Prof. Mahta Moghaddam.
Organized and hosted by Jae-Won Nam.