

40+Gb/s PAM4 Photonic Microring Resonator-Based Transceiver Circuits

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Abstract: Increased data rates have motivated the investigation of advanced modulation schemes, such as four-level pulse-amplitude modulation (PAM4), in optical interconnect systems in order to enable longer transmission distances and operation with reduced circuit bandwidth relative to non-return-to-zero (NRZ) modulation. Employing this modulation scheme in interconnect architectures based on high-Q silicon photonic microring resonator devices, which occupy small area and allow for inherent wavelength-division multiplexing (WDM), offers a promising solution to address the dramatic increase in datacenter and high-performance computing system I/O bandwidth demands. Two ring modulator device structures are proposed for PAM4 modulation, including a single phase shifter segment device driven with a multi-level PAM4 transmitter and a two-segment device driven by two simple NRZ (MSB/LSB) transmitters. Transmitter circuits which utilize segmented pulsed-cascode high swing output stages are presented for both device structures. Output stage segmentation is utilized in the single-segment device design for PAM4 voltage level control, while in the two-segment design it is used for both independent MSB/LSB voltage levels and impedance control for output eye skew compensation. The 65nm CMOS transmitters supply a 4.4Vppd output swing for 40Gb/s operation when driving depletion-mode microring modulators implemented in a 130nm SOI silicon photonic process, with the single- and two-segment designs achieving 3.04 and 4.38mW/Gb/s, respectively. A 56Gb/s PAM4 optical receiver front-end is also described which employs a large input-stage feedback resistor transimpedance amplifier (TIA) cascaded with an adaptively tuned continuous-time linear equalizer (CTLE) for improved sensitivity. Receiver linearity, critical in PAM4 systems, is achieved with a peak-detector-based automatic gain control (AGC) loop.

Biography: Samuel Palermo (S'98-M'07) received the B.S. and M.S. degrees in electrical engineering from Texas A&M University, College Station, TX in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA in 2007. From 1999 to 2000, he was with Texas Instruments, Dallas, TX, where he worked on the design of mixed-signal integrated circuits for high-speed serial data communication. From 2006 to 2008, he was with Intel Corporation, Hillsboro, OR, where he worked on high-speed optical and electrical I/O architectures. In 2009, he joined the Electrical and Computer Engineering Department of Texas A&M University where he is currently an associate professor. His research interests include high-speed electrical and optical interconnect architectures, high performance clocking circuits, and integrated sensor systems. Dr. Palermo is a recipient of a 2013 NSF-CAREER award. He is a member of Eta Kappa Nu and IEEE. He has served as an associate editor for IEEE Transactions on Circuits and System – II from 2011 to 2015 and has served on the IEEE CASS Board of Governors from 2011 to 2012. He is currently a distinguished lecturer for the IEEE Solid-State Circuits Society. He was a coauthor of the Jack Raper Award for Outstanding Technology-Directions Paper at the 2009 International Solid-State Circuits Conference, the Best Student Paper at the 2014 Midwest Symposium on Circuits and Systems, and the Best Student Paper at the 2016 Dallas Circuits and Systems Conference. He received the Texas A&M University Department of Electrical and Computer Engineering Outstanding Professor Award in 2014 and the Engineering Faculty Fellow Award in 2015.



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