USC Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

Ming Hsieh Institute Seminar Series
Ming Hsieh Department of Electrical Engineering
Computer Engineering

Architecture and Runtime for Scalable Quantum Computers

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Quantum computing promise exponential speedups for a class of important problems. However, this potential can be realized only by large-scale quantum systems that operate on a large number of qubits. Unfortunately, to build a scalable quantum computer several challenges must be overcome, including the design of conventional computing and memory systems that can effectively interface with the quantum substrate while obeying the thermal and power constraints dictated by the quantum devices. In this, talk, I will discuss some of our recent work in addressing the design challenges for the control computer for scalable quantum computers.

First, I will discuss our QuEST architecture from MICRO-50 that deals with taming the instruction bandwidth of quantum computers via hardware-managed Error Correction. Qubits are fickle and require continuous error correction. This can require an instruction bandwidth that must scale linearly with the number of qubits and can limit the scalability if error correction is managed in software. QuEST delegates the task of error correction to the hardware and uses programmable microcode to reduce the instruction bandwidth requirements. Second, I will discuss the feasibility of using DRAM-based memory system for Quantum Computers. Quantum computers will require significant memory that can operate at cryogenic temperatures. We characterized commodity DRAM at cryogenic environments and examined the minimum operating temperatures and nature of faults. Finally, I will discuss our upcoming work at ASPLOS 2019 that exploits variation in device error rate to improve the overall reliability of near-term quantum computers.

Moinuddin Qureshi is a Professor of Electrical and Computer Engineering at the Georgia Institute of Technology. His research interests include computer architecture, memory systems, hardware security, and quantum computing. Previously, he was a research staff member (2007-2011) at IBM T.J. Watson Research Center, where he developed the caching algorithms for Power-7 processors. He is a member of the Hall of Fame for ISCA, MICRO, and HPCA. His research has been recognized with the best paper award at MICRO 2018, best paper award at HiPC, and two selections (and three honorable mentions) at IEEE MICRO Top Picks. His ISCA 2009 paper on Phase Change Memory was awarded the 2019 Persistent Impact Prize in recognition of "exceptional impact on the fields of study related to non-volatile memories". He was the Program Chair of MICRO 2015 and Selection Committee Co-Chair of Top Picks 2017. He received his Ph.D. (2007) and M.S. (2003) from the University of Texas at Austin