USC Viterbi
School of Engineering
Ming Hsieh Department of Electrical and Computer Engineering

Ming Hsieh Institute Seminar Series

Computer Engineering

Machine Learning for Performance and Power Modeling/Prediction

Lizy Kurian John
UT Austin

Friday, February 28th, 2020
10:30am-12:00pm
RTH 105

Abstract: Estimating the power and thermal characteristics of SoCs is essential for designing its power delivery system, packaging, cooling, and power/thermal management schemes. Power models that estimate the power consumption of each functional unit/hardware component from first principles are slow and tedious to build. Machine learning can be used to create power models that are fast and reasonably accurate. Machine learning can also be used to calibrate analytical models that estimate power. In this talk, I'll present some examples of performance and power modeling using machine learning.

Another application for machine learning has been to create max power stressmarks. Manually developing and tuning so called stressmarks is extremely tedious and time-consuming while requiring an intimate understanding of the processor. In our past research, we created a framework that uses machine learning for the automated generation of stressmarks. In this talk, the methodology of the creation of automatic stressmarks will be explained. Experiments on multiple platforms validating the proposed approach will be described.

Yet another application for machine learning is in cross-platform performance and power prediction. If one model is slow to run real-world benchmarks/workloads, is it possible to predict/estimate the performance/power by using runs on another platform? Are there correlations that can be exploited using machine learning to make cross-platform performance and power predictions? A methodology to perform cross-platform performance/power predictions will be presented in this talk.

Bio: Lizy Kurian John is Cullen Trust for Higher Education Endowed Professor in the Electrical and Computer Engineering at the University of Texas at Austin. She received her Ph. D in Computer Engineering from the Pennsylvania State University. Her research interests include workload characterization, performance evaluation, memory systems, reconfigurable architectures, and high-performance architectures for emerging workloads. She is recipient of many awards including The Pennsylvania State University Outstanding Engineering Alumnus 2011, the NSF CAREER award, UT Austin Engineering Foundation Faculty Award, Halliburton, Brown and Root Engineering Foundation Young Faculty Award 2001, University of Texas Alumni Association (Texas Exes) Teaching Award 2004, , etc. She has coauthored books on Digital Systems Design using VHDL (Cengage Publishers, 2007, 2017), a book on Digital Systems Design using Verilog (Cengage Publishers, 2014) and has edited 4 books including a book on Computer Performance Evaluation and Benchmarking. In the past, she has served as Associate Editor of IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Computer Architecture Letters, ACM Transactions on Architecture and Code Optimization, and IEEE Micro. She is currently the Editor-in-Chief of IEEE Micro. She holds 12 US patents and is an IEEE Fellow (Class of 2009).