USC Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

Ming Hsieh Institute Seminar Series
Ming Hsieh Department of Electrical Engineering

Integrated Systems

Exploring New Dimensions of CMOS Deep Learning Accelerators with Neural CPU Architecture and Compute-in-Memory Circuits

Jie Gu

Northwestern University

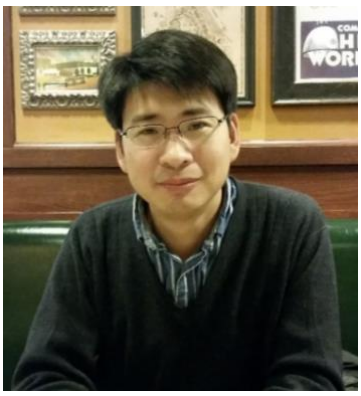
Location: EEB132 & Zoom
2:00 pm – 3:30 pm, Friday, Dec. 3rd, 2021

Meeting ID: 947 0191 2463 Passcode:138956

https://usc.zoom.us/j/94701912463?pwd=eW1KVmhuODFHdHpMemhQbTllMEZ6Zz09

Abstract: As Moore's law stalls, novel architecture and circuit solutions are urgently needed to meet the ever-growing computing demands from emerging artificial intelligence (AI) applications on resource-constrained edge devices. This talk will elaborate our efforts in exploring new dimensions of circuit and architecture solutions. First, we will discuss our recent developments of a special "neural CPU" architecture in conjunction of Von-Neumann and Neuromorphic design, where a deep neural network accelerator is reconfigured to perform RISC-V CPU showing significant benefits in computing performance and silicon cost. Second, we will discuss our developments on compute-in-memory circuits with mixed-signal computing where time-domain circuits and analog memory are utilized to achieve a state-of-art computing efficiency. Demonstrations of test chips with standard CMOS process will be used to show the benefits of the proposed architecture and circuits in comparison with the conventional implementation.

Biography: Jie Gu is currently an associate professor in Northwestern University. He received his B.S. degree from Tsinghua University, M.S. degree from Texas A&M University and Ph.D. degree from University of Minnesota. From 2008 to 2010, he was with Texas Instruments, Dallas, TX on research and developments of ultra-low voltage mobile processors for smartphones. From 2011 to 2014, he was with Maxlinear leading developments of home multi-media broadband SoC chips. He joined ECE department in Northwestern University from 2015 working on novel circuit and architecture for low power microprocessors and machine learning accelerators. He is a recent recipient of NSF CAREER award.



Faculty Hosts: Mike Chen, Hossein Hashemi, Manuel Monge, Constantine Sideris

Student Organizer & Host: Qiaochu Zhang (qiaochuz@usc.edu)