USC Viterbi School of Engineering
Ming Hsieh Department of Electrical and Computer Engineering

Seminar

Efficient On-chip Neural Architecture and Data Processing in the Era of Domain-specific Computing and AI

Jie Gu

Associate Professor - Department of ECE
Northwestern University

Monday, April 11, 2022
9:00am via Zoom

Zoom link: https://usc.zoom.us/j/93576256328?pwd=OUlzMFYxVzVTY1cwNit5NFR6Nmdmdz09
Meeting ID: 935 7625 6328 Passcode: 877156

Abstract: In this new era of data-driven domain-specific computing, the integrated circuits, serving as the cornerstones of modern electronic devices, are facing tremendous challenges in meeting the ever-growing data processing demand under staggering technology improvement. It is clear that conventional Von-Neumann architecture is no longer sufficient for the ubiquitous AI and many newly-arrived complex computing tasks. As a result, it is critical to look for new computing architecture that delivers the most efficient computing and data processing solutions. In this talk, I will first discuss our recent developments of a special "neural CPU" processor at the conjunction of Von-Neumann and deep learning architectures to establish a new computing platform where general-purpose computing is incorporated into the framework of deep learning accelerators achieving significant end-to-end performance enhancement and data movement reduction. Second, I will discuss efficient data processing solutions for domain-specific computing using examples of a sparse convolutional neural network accelerator for 3D/4D point-cloud image classification and efficient data processing for wirelessly powered human machine interface System-on-Chip (SoC) with embedded machine learning capabilities. Demonstrations of test chips using standard CMOS process will be used to show the benefits of the proposed solutions in comparison with the conventional implementations.

Biography: Jie Gu is currently an associate professor in Northwestern University. He received his B.S. degree from Tsinghua University, M.S. degree from Texas A&M University and Ph.D. degree from University of Minnesota. From 2008 to 2010, he was with Texas Instruments, Dallas, TX on research and developments of ultra-low voltage mobile processors for smartphones. From 2011 to 2014, he was with Maxlinear leading developments of home multi-media broadband SoC chips. He joined ECE department in Northwestern University from 2015 working on novel circuit and architecture for low power microprocessors and machine learning accelerators. He is a recent recipient of NSF CAREER award.