



Devices & ASICs for Machine Intelligence and Post-Quantum Cryptography

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EEB 248 @ 2pm
And Via Zoom

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Meeting ID: 931 0939 8818 Passcode: 540610

Abstract: The high demand for AI services in conjunction with a dramatic chip shortage along with technology leaps such as 5/6G networks, cybersecurity threats, and quantum algorithms have resurrected a R&D push for advanced devices, information processing, and computing capability. To address this demand and explore novel technology, unique opportunities exist, for example, given by algorithmic parallelism of mixed-signal non-van Neuman accelerators. Especially electronic-photonics ASIC compute paradigms hold promise to enable non-iterative $O(1)$ runtime complexity, ps-short latency, and TOPS/W throughputs. This opens prospects for next-generation hardware both for AI cloud services but also for accelerating edge computing such as enabled by compact and efficient PIC-CMOS co-designs pushing the SWAP envelope. As both a professor and a co-founder of a venture, in this seminar I will share my latest insights on fundamental complexity scaling and algorithm-hardware homomorphism on the one hand, and device- circuit- and system-level demonstrations on the other. I will introduce a novel memristive photonic RAM capable of zero-static power consumption suitable for AI edge applications and highlight our photonic tensor core ASIC demonstration leveraging parallelism including a software stack. Beyond matrix-matrix multiplication acceleration, I will show our Convolution Theorem-based accelerator enabling 1000x1000 matrix-size convolutions at 100us latency, or about 10x faster than today's GPUs. At the device level I will share advanced optoelectronics and quantum matter including a 50Gbps ITO-based modulator being 1,000x more compact than Silicon PDK solutions, discuss strainoptronic detectors with high gain-bandwidth-product, a 100GHz fast VCSEL, and share a path for an electrically-driven quantum source. Finally, having solved the complex-signal convolution I will show a Montgomery Multiplier for a data-center RSA public-key cryptosystem, and conclude by highlighting our recent post-quantum secure-hash-algorithm (SHA) system accelerating blockchain operations. I will conclude with an R&D outlook for the next decade and share examples of my passion supporting values and programs on diversity & inclusion.

Biography: Volker J. Sorger is an Associate Professor in the Department of Electrical and Computer Engineering and the Director of the *Institute on AI & Photonics*, the Head of the *Devices & Intelligent Systems Laboratory* at the George Washington University. His research areas include devices & optoelectronics, AI/ML accelerators, mixed-signal ASICs, quantum matter & processors, and cryptography. For his work, Dr. Sorger received multiple awards including the Presidential PECASE Award, the AFOSR YIP Award, the Emil Wolf Prize, and the National Academy of Sciences award of the year. Dr. Sorger is an Associate editor for OPTICA, serves on the board of Chip, and was the former editor-in-chief of Nanophotonics. He is a [Fellow of Optica](#) (former OSA), a [Fellow of SPIE](#), a Fellow of the German National Academic Foundation, and a Senior Member of IEEE. He is a co-founder of [Optelligence](#) Company.