

Integrated Systems

Ising-Memory: Advancing Combinatorial Optimization Accelerators with Ising Computations in Memory

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Date: Friday, September 9th, 2022 - Time: 2:00pm -Location: EEB 132
Refreshments will be served

Abstract: Combinatorial optimization problems (COPs) find applications in real-world scientific, industrial, and societal scenarios. Such COPs are computationally NP-hard, and an exhaustive brute force search for the optimal solution becomes untenable as the COP size increases. To expedite the COP computation, the Ising model formalism is used, which abstracts spin dynamics in a ferromagnet. The spins are orientated to reach the minimum energy state, representing the optimum COP solution. Previous Ising engine designs utilized dedicated annealing processors or additional digital arithmetic circuits next to the memory bitcells. These custom circuits or processors cannot be repurposed for other applications, incurring significant area and power overhead.

In this seminar, I will present a reconfigurable and scalable compute-within-memory analog approach for Ising computation. This area-efficient approach repurposes existing embedded memory bitcell columns and peripheral circuits to perform analog domain Hamiltonian calculations on the bitlines, significantly minimizing area and power overhead. I will present the Silicon hardware results and discuss how the Ising-Memory approach can be adopted in various classes of optimization problems such as SAT solvers and Integer linear programming.

Biography:



Dr. Jaydeep Kulkarni received a B.E. degree from the University of Pune, India, in 2002, an M. Tech degree from the Indian Institute of Science (IISc) in 2004, and a Ph.D. degree from Purdue University in 2009. During 2009-2017, he worked as a Research Scientist at Intel Circuit Research Lab in Hillsboro, OR. Currently, he is an assistant professor in the department of electrical and computer engineering at the University of Texas at Austin, a fellow of Silicon Labs Chair in electrical engineering, and a fellow of AMD chair in computer engineering. Dr. Kulkarni has filed 36 patents, published two book chapters, and 100+ papers in refereed journals and conferences. His research is focused on machine learning hardware accelerators, in-memory computing, emerging nano-devices, heterogeneous and 3D integrated circuits, hardware security, and cryogenic computing.

Dr. Kulkarni received the best M. Tech student award from IISc Bangalore, Intel Foundation Ph.D. fellowship award, Purdue School of ECE outstanding doctoral dissertation award, IEEE Transactions on VLSI systems best paper award, SRC outstanding industrial liaison award, Micron Foundation Faculty Awards, Intel Rising Star Faculty Award and the NSF CAREER Award. He is a senior member of IEEE and the U.S. National Academy of Inventors.

Research Group: Circuit Research Lab, <https://sites.utexas.edu/CRL/>.

Hosted by Prof. Hossein Hashemi, Prof. Mike Chen and Prof. Constantine Sideris
Organized and hosted by Vinay Chenna (vchenna@usc.edu).