



## Agile Design of Domain-Specific Accelerators and Compilers

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**EEB 248**

**<https://usc.zoom.us/j/93842345540?pwd=V3U1TUgwK2pyTE9BWThDeCtXbDJOdz09>**  
**Meeting ID: 938 4234 5540    Passcode: 051562**

**Abstract:** With the slowing of Moore's law, computer architects have turned to domain-specific hardware accelerators to improve the performance and efficiency of computing systems. However, programming these systems entails significant modifications to the software stack to properly leverage the specialized hardware. Moreover, the accelerators become obsolete quickly as the applications evolve. What is needed is a structured approach for generating programmable accelerators and for updating the software compiler as the accelerator architecture evolves with the applications. In this talk, I will describe a new agile methodology for co-designing programmable hardware accelerators and compilers. Our methodology employs a combination of new programming languages and formal methods to automatically generate the accelerator hardware and its compiler from a single specification. This enables faster evolution and optimization of accelerators, because of the availability of a working compiler. I will showcase this methodology using Amber, a coarse-grained programmable accelerator for imaging and machine learning (ML) we designed and fabricated using our flow in TSMC 16 nm technology. I will show how we agilely evolved Amber into Onyx, our next generation accelerator, using an application-driven design space exploration framework called APEX enabled by our hardware-compiler co-design flow.



**Bio:** Priyanka Raina is an Assistant Professor of Electrical Engineering at Stanford University. She received her B.Tech. degree in Electrical Engineering from the IIT Delhi in 2011 and her S.M. and Ph.D. degrees in Electrical Engineering and Computer Science from MIT in 2013 and 2018. Priyanka's research is on creating high-performance and energy-efficient architectures for domain-specific hardware accelerators in existing and emerging technologies. She also works on methodologies for agile hardware-software co-design. Her research has won best paper awards at VLSI, ESSCIRC and MICRO conferences and in the JSSC journal. She has also won the NSF CAREER Award, the Intel Rising Star Faculty Award, Hellman Faculty Scholar Award and is a Terman Faculty Fellow.

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