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Ming Hsieh Department of Electrical and Computer Engineering

Novel Materials for Next-Generation Electronics: From Low-Power to Extreme Environment Computing



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Abstract: Silicon has been the dominant material for electronic computing for decades and very likely will stay dominant for the foreseeable future. However, it is well-known that Moore's law that propelled Silicon into this dominant position is long dead. Therefore, a fervent search for (i) new semiconductors that could directly replace silicon or (ii) new architectures with novel materials/devices added onto silicon or (iii) new physics/state-variables or a combination of above has been the subject of much of the electronic materials and devices research of the past 2 decades. The above problem is further complicated by the changing paradigm of computing from arithmetic centric to data centric in the age of billions of internet-connected devices and artificial intelligence as well as the ubiquity of computing in ever more challenging environments. Therefore, there is a pressing need for complementing and supplementing Silicon to operate with greater efficiency, speed and handle greater amounts of data. This is further necessary since a completely novel and paradigm changing computing platform (e.g. all optical computing or quantum computing) remains out of reach for now.

The above is however not possible without fundamental innovation in new electronic materials and devices. Therefore, in this talk, I will try to make the case of how novel layered two-dimensional (2D) chalcogenide materials¹ and threedimensional (3D) nitride materials might present interesting avenues to overcome some of the limitations being faced by Silicon hardware. I will start by presenting our ongoing and recent work on integration of 2D chalcogenide semiconductors with silicon² to realize low-power tunnelling field effect transistors. In particular I will focus on In-Se based 2D semiconductors² for this application and extend discussion on them to phase-pure, epitaxial thin-film growth over wafer scales,³ at temperatures low-enough to be compatible with back end of line (BEOL) processing in Silicon fabs.

I will then switch gears to discuss memory devices from 2D materials when integrated with emerging wurtzite structure ferroelectric nitride materials⁴ namely aluminium scandium nitride (AlScN). First, I will present on Ferroelectric Field Effect Transistors (FE-FETs) made from 2D materials when integrated with AlScN and make the case for 2D semiconductors in this application.⁵⁻⁷ I will then switch resistive memory devices made from AIScN termed Ferrodiodes (FeDs)⁸ which show multi-bit operation⁹ as well as compute in memory (CIM)¹⁰. Finally, I will make a case as to why AlScN FeDs are uniquely suited as a high temperature non-volatile memory demonstrating stable operation upto 600 C^{11} and how AlScN can be integrated onto SiC¹² for stable data retention in ferroelectric capacitors upto 800 C.¹³ I will end by providing a broad outlook on both AI computing hardware as well as high-temperature computing.¹⁴

References:

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Bio: Deep Jariwala is an Associate Professor and the Peter & Susanne Armstrong Distinguished Scholar in the Electrical and Systems Engineering as well as Materials Science and Engineering at the University of Pennsylvania (Penn). Deep completed his undergraduate degree in Metallurgical Engineering from the Indian Institute of Technology in Varanasi and his Ph.D. in Materials Science and Engineering at Northwestern University. Deep was a Resnick Prize Postdoctoral Fellow at Caltech before joining Penn to start his own research group. His research interests broadly lie at the intersection of new materials, surface science and solid-state devices for computing, opto-electronics and energy harvesting applications in addition to the development of correlated and functional imaging techniques. Deep's research has been widely recognized with several awards from professional societies, funding bodies, industries as well as private foundations, the most notable ones being the Optica Adolph Lomb Medal, the Bell Labs Prize, the AVS Peter Mark Memorial Award, IEEE Photonics Society Young Investigator Award, IEEE Nanotechnology Council Young Investigator Award, IUPAP Early Career Scientist Prize in Semiconductors, the SPIE Early career achievement award and the Alfred P. Sloan Fellowship. He has published over 150 journal papers with more than 22000 citations and holds several patents. He serves as the Associate Editor for ACS Nano Letters and has been appointed as a Distinguished Lecturer for the IEEE Nanotechnology Council for 2025.

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