Synthesizing RFICs from Digital Standard Cell Libraries

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RF front-end circuits designed today for operation in the 1 to 10GHz range are almost exclusively fabricated in CMOS processes. This includes low-noise and power amplifiers, mixers, oscillators, A/D converters… all the components that allow radios to communicate wirelessly. Traditional design of these RF components relies on precise RF models, high-quality passives, and time-consuming custom layout for matching and controlled signal paths. The basic building blocks used to realize these RF components are, not surprisingly: transistors, resistors, inductors, and capacitors.

CMOS logic has become so fast, it is now realistic to design logic using full-swing CMOS standard cell libraries that switch at >10GHz speeds. CMOS logic has become so small; we can now fit 1000’s of gates in the area occupied by a single inductor. As RF circuit designers, we can think about how to accomplish the same functionality of an RF front-end, but do so with a new set of basic building blocks: NAND, tri-state buffers, flip-flops, etc. This could allow us to describe RF circuits as a netlist of only logic gates, which in-turn enables fully automated layout with digital CAD tools. Benefits include shorter design cycles and reduced chip area, which will continue to shrink with process scaling. With smaller area also comes lower power. This talk will present several implementations of all-digital RF circuits synthesized from digital standard cell libraries. A UWB transmitter, time-to-digital converter, and PLL in 65nm CMOS will be presented. The core tuning structures and the calibration technique will be described, which allows the circuits to be precisely regulated over process, voltage, and temperature variations.

Biography: David D. Wentzloff received the B.S.E. degree in Electrical Engineering from the University of Michigan, Ann Arbor, in 1999, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, in 2002 and 2007, respectively. In the summer of 2004, he worked in the Portland Technology Development group at Intel in Hillsboro, OR. Since August, 2007 he has been with the University of Michigan, Ann Arbor, where he is currently an Assistant Professor of Electrical Engineering and Computer Science. He is the recipient of the 2002 MIT Masterworks Award, 2004 Analog Devices Distinguished Scholar Award, 2009 DARPA Young Faculty Award, the 2009-2010Eta Kappa Nu Professor of the Year Award, and the 2011 DAC/ISSCC Student Design Contest Award. He has served on the technical program committee for ICUWB 2008-2010 and ISLPED 2011, and as a guest editor for the IEEE T-MTT, the IEEE Communications Magazine, and the Elsevier Journal of Signal Processing: Image Communication. He is a member of IEEE, IEEE Circuits and Systems Society, IEEE Microwave Theory and Techniques Society, IEEE Solid-State Circuits Society, and Tau Beta Pi.

Date: Friday November 11th, Time: 3 - 4:30PM, Location: EEB 248