This presentation describes the design of the architecture and circuit blocks for backplane communication transceivers. A channel study investigates the major challenges in the design of high-speed reconfigurable transceivers. Architectural solutions resolving channel-induced signal distortions are proposed and their effectiveness on various channels is investigated. Subsequently, the presentation describes the design of two fully-adaptive backplane transceivers embedded in state-of-the-art low-leakage 28nm CMOS FPGAs operating up to 12.5Gb/s and 13.1Gb/s. The receive AFE utilizes a three-stage CTLE to provide selective frequency boost for long-tail ISI cancellation. A speculative DFE removes the immediate post-cursor ISI. The second transceiver also uses a 4-tap sliding DFE to remove the post-cursor ISI up to 64 taps. Both CTLE and DFE are fully adaptive using sign-sign LMS algorithm. A novel clocking technique uses wideband LC and ring oscillators for reliable clocking for 0.6-12.5Gb/s and 0.6-13.1Gb/s operation. The transmitter utilizes a 3-tap FIR and provides flexibility for supply and ground referenced operation. The two transceivers achieve BER < 10^{-15} over a 33dB-loss backplane at 12.5Gb/s, and over a 31dB-loss backplane at 13.1Gb/s. Both transceivers achieve BER < 10^{-15} over channels with 10G-KR characteristics at 10.3125Gb/s.

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