Generating precise clocks using clumsy transistors available in highly-scaled CMOS technologies is a challenging task. In this talk, several architectural- and circuit-level techniques that seek to overcome the detrimental impact of analog circuit imperfections that plague conventional clock generators will be discussed. After a brief overview of the drawbacks of classical analog phase-locked loops (PLLs), the talk progresses with the evolutionary presentation of highly digital clock generators. Several case studies of digital PLLs that achieve sub-ps absolute jitter, better than 1mW/GHz power efficiency and very wide operating range will be presented. Application of digital PLLs for supply noise cancellation and charge recycling will be outlined.

Biography:  **Pavan Kumar Hanumolu** received the Ph.D. degree in electrical engineering from Oregon State University in 2006. Currently, he is an Assistant Professor in the School of Electrical Engineering and Computer Science at the same University. His research interests include high-speed I/O interfaces, digital techniques to compensate for analog circuit imperfections, time-based signal processing, and power-management circuits.

**Date:** Friday January 27th, **Time:** 2:30 - 4PM, **Location:** EEB 248